Employee Locator
query by organization

14 Records Were Found

Employee	Office	Building	Fl.-Ste./Corr.-Rm	Contact No.	Type	Ext
ANDERSON MATTHEW D	P/2186	PK2	02/B20	(703)306-5931	T	
BATAILLE PIERRE MICHE (PIERRE-MICHE)	P/2186	PK2	02/D08	(703)305-0134	T	
CHOI WOO H	P/2186	PK2	02/A22	(703)305-3845	T	
ELMORE STEPHEN C	P/2186	PK2	02/C19	(703)308-6256	T	
KIM HONG C	P/2186	PK2	02/D10	(703)305-3835	T	
KIM MATTHEW (MATT) M (SPE)	P/2186	PK2	02/R01	(703)305-3821	T	
LI ZHUO H	P/2186	PK2	02/A10	(703)305-3846	T	
PATEL HETUL B	P/2186	PK2	02/A33	(703)305-6219	T	
PEIKARI BEHZAD	P/2186	PK2	02/Y11	(703)305-3824	T	
ROBERTSON DAVID (DAVID L.) L	P/2186	PK2	02/Y09	(703)305-3825	T	
SHAH SAUMIL R	P/2186	PK2	03/C22	(703)305-8786	T	
THAI TUAN V	P/2186	PK2	02/R11	(703)305-3842	T	
THOMAS SHANE M	P/2186	PK2	02/A08	(703)605-0725	T	
TRAN DENISE	P/2186	PK2	02/R03	(703)305-9823	T	

Contact Number Type: T - Telephone, F - Fax, R - Receptionist, P - Pager, M - Mobile

Reg Brag Don

Employee Search Completed
No more records to search

(*) Memory Accessing, Addressing.

Class 711 ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY

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1	**ADDRESSING COMBINED WITH SPECIFIC MEMORY CONFIGURATION OR SYSTEM**
2	. Addressing extended or expanded memory
3	. Addressing cache memories
4	. Dynamic-type storage device (e.g., disk, tape, drum)
5	. For multiple memory modules (e.g., banks, interleaved memory)
6	. Virtual machine memory addressing
100	**STORAGE ACCESSING AND CONTROL**
101	. Specific memory composition
102	.. Solid-state read only memory (ROM)
103	... Programmable read only memory (PROM, EEPROM, etc.)
104	.. Solid-state random access memory (RAM)
105	... Dynamic random access memory
106	.... Refresh scheduling
107	.. Ferrite core
108	.. Content addressable memory (CAM)
109	.. Shift register memory
110	... Circulating memory
111	.. Accessing dynamic storage device
112	... Direct access storage device (DASD)
113	.... Caching
114	.... Arrayed (e.g., RAIDs)
115	.. Detachable memory
116	.. Bubble memory
117	. Hierarchical memories
118	.. Caching
119	... Multiple caches
120	.... Parallel caches
121	.... Private caches
122	.... Hierarchical caches
123	.... User data cache and instruction data cache
124	.... Cross-interrogating
125	... Instruction data cache
126	... User data cache
127	... Interleaved
128	... Associative
129	... Partitioned cache

130 ... Shared cache
131 ... Multiport cache
132 ... Stack cache
133 ... Entry replacement strategy
134 .... Combined replacement modes
135 .... Cache flushing
136 .... Least recently used
137 ... Look-ahead
138 ... Cache bypassing
139 .... No-cache flags
140 ... Cache pipelining
141 ... Coherency
142 .... Write-through
143 .... Write-back
144 .... Cache status data bit
145 .... Access control bit
146 .... Snooping
147 . Shared memory area
148 .. Plural shared memories
149 .. Multiport memory
150 .. Simultaneous access regulation
151 .. Prioritized access regulation
152 .. Memory access blocking
153 .. Shared memory partitioning
154 . Control technique
155 .. Read-modify-write (RMW)
156 .. Status storage
157 .. Interleaving
158 .. Prioritizing
159 .. Entry replacement strategy
160 ... Least recently used (LRU)
161 .. Archiving
162 ... Backup
163 .. Access limiting
164 ... With password or key
165 .. Internal relocation
166 .. Resetting
167 . Access timing
168 .. Concurrent accessing
169 .. Memory access pipelining
170 . Memory configuring
171 .. Based on data size
172 .. Based on component size
173 .. Memory partitioning
200 ADDRESS FORMATION
201 . Slip control, misaligning, boundary alignment
202 . Address mapping (e.g., conversion, translation)

203	.. Virtual addressing
204	... Predicting, look-ahead
205	.... Directories and tables (e.g., DLAT, TLB)
206	... Translation tables (e.g., segment and page table or map)
207	.... Directory tables (e.g., DLAT, TLB)
208	.... Segment or page table descriptor
209	... Including plural logical address spaces, pages, segments, blocks
210	.. Resolving conflict, coherency, or synonym problem
211	. Address multiplexing or address bus manipulation
212	. Varying address bit-length or size
213	. Generating prefetch, look-ahead, jump, or predictive address
214	. Operand address generation
215	. In response to microinstruction
216	. Hashing
217	. Generating a particular pattern/sequence of addresses
218	.. Sequential addresses generation
219	. Incrementing, decrementing, or shifting circuitry
220	. Combining two or more values to create address
221	. Using table

FOREIGN ART COLLECTIONS

FOR000 **CLASS-RELATED FOREIGN DOCUMENTS**

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